REMARKS

Claims 1-6, 8 and 11-15 are all the claims pending in the application.

Claim Rejections - 35 U.S.C. § 102(b)

The Examiner has rejected claims 1-6, 8, and 11-15 under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 5,982,680 to Wada et al. (hereinafter "Wada"). Applicants submit that the claims are patentable.

For example, claim 1 recites a semiconductor memory device which includes a plurality of memory blocks, and a plurality of redundancy memory blocks provided for each of the plurality of memory blocks. Each of the plurality of memory blocks includes a plurality of segments which are adjacent to one after another. Segments having defects among the plurality of segments in a memory block among the plurality of memory blocks are sequentially allocated to the plurality of redundancy memory blocks and replaced by the allocated redundancy memory blocks.

Wada is directed to a semiconductor memory cell 12 which comprises a plurality of sub-block columns A, B, C, and D (See Figure 10). Each sub-block column includes a plurality of sub-blocks 21 which may be grouped in groups of 2 to 2^n blocks 51. Each sub-block column A, B, C, and D is provided with a redundancy memory 48 (col. 9, lines 24-25). Each redundancy memory 48 is provided with blocks 54 which are allocated in a corresponding one-to-one manner to blocks 51 (col. 10, lines 55-59 and col. 12, lines 9-13). Additional blocks 54 of the redundancy memory 48 are left unused (abstract and col. 13, lines 7-12).

In framing the rejection, the Examiner does not clearly indicate which elements of Wada allegedly correspond to the claimed plurality of memory blocks or the claimed plurality of redundancy memory blocks. It seems that the Examiner contends that Wada's sub-block columns A, B, C, and D which comprise blocks 51 correspond to the claimed plurality of memory blocks which include a plurality of segments. It also seems that the Examiner contends that Wada's redundancy memory 48 corresponds to the claimed plurality of redundancy blocks.

However, Wada discloses that each redundancy memory 48 is provided with blocks 54 which are allocated in a corresponding one-to-one manner to blocks 51 (col. 10, lines 55-59 and col. 12, lines 9-13). Clearly, blocks 51 which have errors are only allocated to blocks 54 in the redundancy memory 48 of the same sub-block column A, B, C, or D. In other words, blocks 51 in sub-block column A are only allocated to the blocks 54 in redundancy memory 48 of sub-block column A. Likewise, blocks 51 in sub-block columns B, C, and D are only allocated to the blocks 54 in the redundancy memory 48 within the respective sub-bloc columns. Thus, Wada does not teach or suggest that the alleged segments having defects (blocks 51) among the plurality of segments in the alleged memory block (e.g., sub-block column A) among the plurality of memory blocks are sequentially allocated to the alleged *plurality* of redundancy memory blocks (sub-block columns A, B, C, and D) and replaced by the allocated redundancy memory blocks.

Because Wada does not teach or suggest all of the features of claim 1, Applicants submit that the claim is not anticipated by Wada. Applicants also submit that claims 2-4, being dependent on claim 1, are patentable at least by virtue of their dependency.

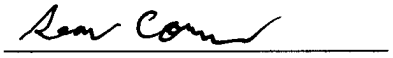
Independent claims 5 and 6 recite features similar to those discussed above in conjunction with claim 1. Thus, Applicants submit that these claims are patentable at least for reasons analogous to those discussed above regarding claim 1. Applicants also submit that claims 6, 8, and 11-15, being dependent on one of claims 5 and 6, are patentable at least by virtue of their dependency.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Date: March 3, 2008